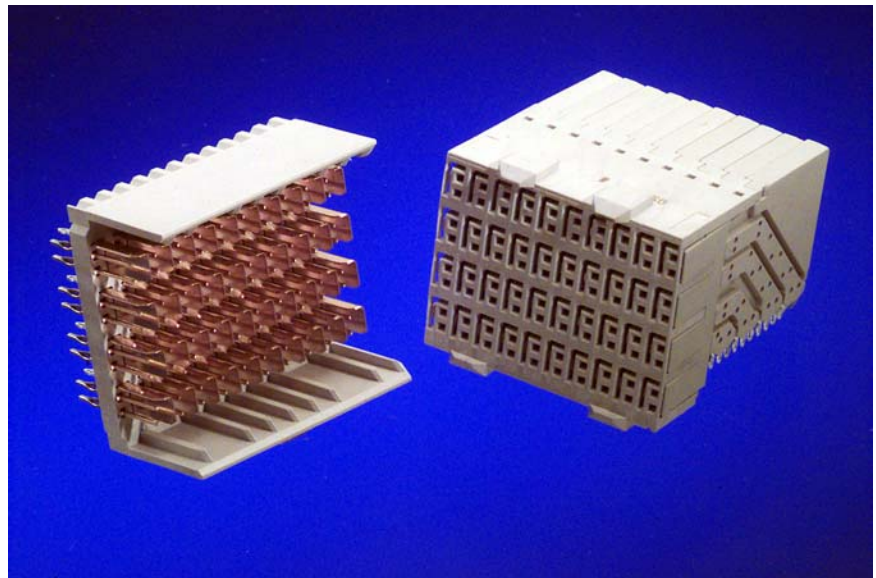


## 10 Gigabit Ethernet

Positioned as a high-speed, unifying technology for networking applications in LANs, MANs, and WANs, 10 Gigabit Ethernet will provide simple, high bandwidth at relatively low cost. In LAN applications, 10 Gigabit Ethernet will enable organizations to scale their packet-based networks from 10 Mbps to 10,000 Mbps, thereby leveraging their investments in Ethernet. In MAN and WAN applications, 10 Gigabit Ethernet will enable service providers and others to create extremely high-speed links at very low cost.



## XAUI HM-Zd Interoperability Platform

- A common platform for interoperability testing supported by members of the 10GEA XAUI Interoperability Group and the 10 Gigabit Ethernet Consortium
- Full duplex link testing
- 3 link lengths
  - 5 inches
  - 20 inches
  - 34 inches
- XAUI signals run in a system-like environment
  - FR-4
  - Multi-layer connections
  - 0.200" backplane thickness
  - MDIO / MDC Support

## Z-PACK HM-Zd

- Fully modular system- standard size is 25 mm
- Available in two versions:
  - 2 signal pairs per column (20 pairs per 25 mm)
  - 4 signal pairs per column (40 pairs per 25 mm)
- Dual beam contact system with fully encompassing grounds
- Robust mating interface with integral prealignment and mating built-in
- Optimized footprint for improved electrical performance

## XAUI Interoperability – Industry Support

The 10 Gigabit Ethernet Alliance has formed a working group, which is chaired by Tyco Electronics, to examine interoperability between different vendors' XAUI implementation. This group selected the Tyco Electronics XAUI HM-Zd Interoperability Platform as a common platform for interoperability testing. The work completed by this group has been adopted by the 10 Gigabit Ethernet Consortium, which will perform future interoperability testing.

BitBlitz has tested their BBT3400 XAUI Interface with the XAUI HM-Zd Interoperability Backplane, and has been able to achieve error free operation at the maximum link length of 34 inches. BitBlitz has summarized this testing in its application support documentation.

For further details regarding the operation of the BitBlitz BBT3400 with the XAUI HM-Zd Interoperability Backplane, please contact BitBlitz Communications at [sales@bitblitzcom.com](mailto:sales@bitblitzcom.com).

## BitBlitz Communications XAUI Product Offerings

- **BBT3400:**  
The BBT3400 is the industry's lowest power, highest performance XAUI-XGMII transceiver. The device is ideal for high bandwidth interconnection between line cards, serial backplanes, or optical modules. In volume shipment today, the BBT3400 dissipates only 200 mW per channel, generates only 2.4 ps RMS random jitter, and links over 40 inch of FR-4 traces.
- **BBT3401:**  
The BBT3401 is the industry's only intelligent XAUI-XAUI retimer. In addition to re-setting jitter, the BBT3401 examines the data content to add/drop IDLE to compensate clock difference. It also deskews across multiple-channels. The BBT3401 dissipates only 200mW per channel, generates only 2.4ps RMS random jitter, and extend driving distance of XAUI link by over 40 inches of FR-4 traces.



## XAUI to XGMII Low Power CMOS 4 Channel 3.125Gbps Transceiver

### Features

- Up to 12.5 Gbps Duplex Raw Data Rate
- Up to 3.125 Gbps per channel
- Compliant with 10-Gigabit Ethernet (IEEE 802.3ae) D.3.1
  - Superior to proposed jitter requirements
- User-Controlled Dual-Speed functionality
  - 3.125 Gbps or 2.5 Gbps
  - 1.56 Gbps or 1.25 Gbps
- Ultra low-power operation
  - 200mW typical per channel
  - 1.8V or 2.5V I/O: 3.3V tolerant
- 8B/10B Encoder/Decoder Ch. (optional)
- XGMII
  - SSTL2 or HSTL 1.8V
  - 8-bit or 10-bit Parallel Input/Output Data
- Comma detection (Both disparities) Byte alignment
  - Programmable “K” character
- Channel-to-Channel Alignment
- Single-ended or differential input Reference clock
- Flexible Tx and Rx Clock Schemes
- Receive Cable Equalization
- Per Channel Signal detect indicator
- Double Data-Rate (DDR) Mode
- 802.3 compliant MDC/MDIO serial interface
- Clock compensation via IDLE insertion, deletion

### Applications

The nPower BBT3400 is a quad 8-bit/10-bit parallel-to-serial and serial-to-parallel transceiver device ideal for high bandwidth interconnection between line cards, serial backplanes, or optical modules. In addition to high-bandwidth links, the transceivers can be configured as a single 10 Gigabit eXtended Attachment Unit Interface (XAUI), providing up to 12.5 Gbps of duplex bandwidth. See Figure 1.

### Benefits

- Industry-leading power performance
- Receiver Equalization eliminates needs to over-drive at transmitter
  - Reduced EMI, cross-talk
- Link distances of up to 40” FR-4 traces and two connectors
- Proven Interoperability with various backplanes, optical modules and semiconductors
- Complete applications collateral
  - Evaluation Board
  - Applications Note
  - Verilog Model
  - SPICE Model
  - High-Speed System Engineering technical support

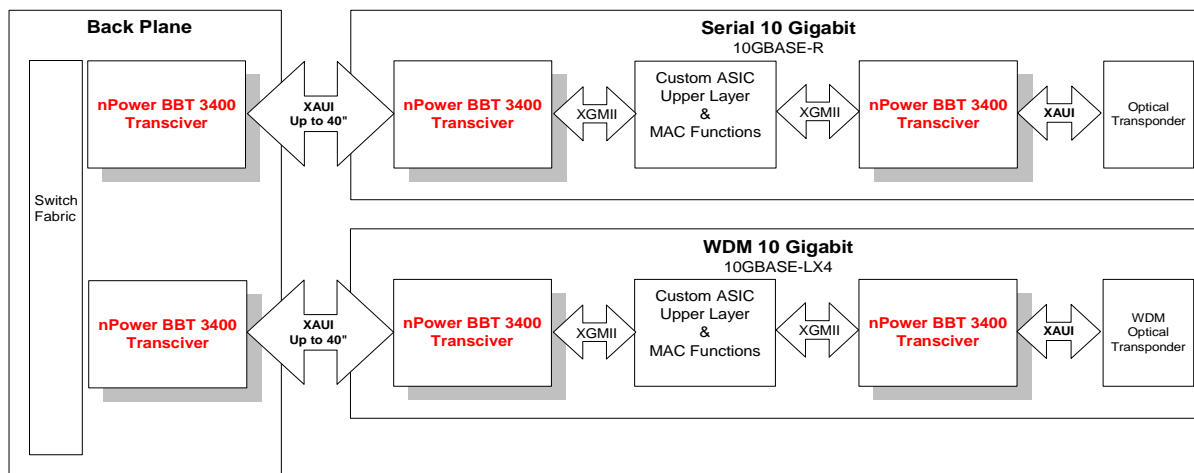


Figure 1 Backplane & Line Card Applications



# nPower BBT3400 Quad 3.125G Transceiver

## Data Flow

The BBT3400 Transmitters normally accept data from the parallel XGMII data bus, clocked by the appropriate Transmit Byte Clock for the channel, and resynchronize it into the Transmit FIFO using local reference clock. The data is then optionally encoded using the standard IEEE802.3-2000 8B/10B encoder, serialized, and sent out on the differential CML, XAUI-compatible Tx pins. The BBT3400 Receivers accept serial data from the CML pins, perform clock and data recovery on the bit stream, optionally scan the data for the “comma” patterns and Byte-Align the data on either ‘disparity’ comma pattern, and de-serialize the data. The data is then optionally 10B/8B decoded into the XGMII data stream, and fed into the receiver FIFO, where clock compensation, optional channel alignment, and resynchronization to any

one of the individual recovered clocks, one channel clock, or the local reference clock are performed.

In addition, several other facilities are provided to ease system testing. Loopback at either the serial or parallel ports is available under external pin or MII control. Suitable control and status registers are available through the IEEE standard MDIO/MDC system. The XGMII interface may be configured in source-centered or source synchronous timing formats for ASIC-friendly timing.

If the Built-in-Self-Test function (BIST) is in use, the serial Tx data instead is derived from a PRBS  $2^{23} - 1$  pattern generator. In this BIST mode, the received serial data is checked against the PRBS pattern transmitted and, if an error is found, a flag signal is provided.

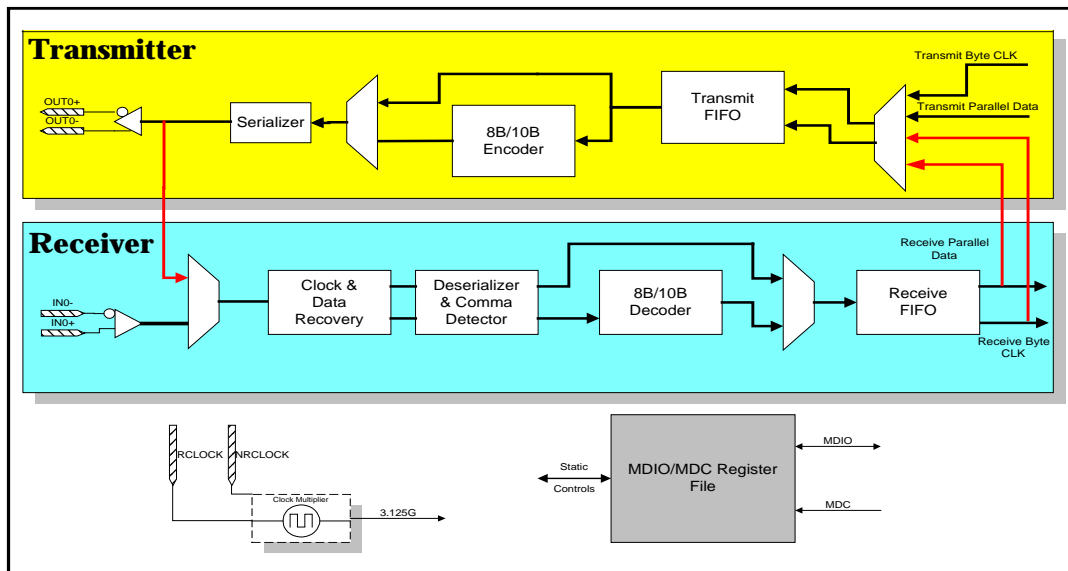


Figure 2 BBT3400 Functional Block Diagram

**Part Ordering Information:**  
nPower BBT3400 – 289-pin BGA

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