

## 10 Gigabit Ethernet

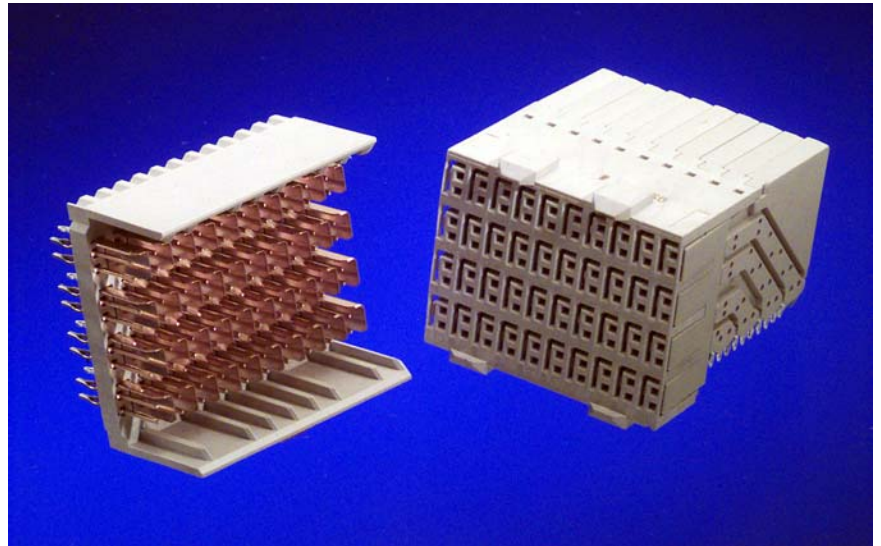
Positioned as a high-speed, unifying technology for networking applications in LANs, MANs, and WANs, 10 Gigabit Ethernet will provide simple, high bandwidth at relatively low cost. In LAN applications, 10 Gigabit Ethernet will enable organizations to scale their packet-based networks from 10 Mbps to 10,000 Mbps, thereby leveraging their investments in Ethernet. In MAN and WAN applications, 10 Gigabit Ethernet will enable service providers and others to create extremely high-speed links at very low cost.

## XAUI HM-Zd Interoperability Platform

- A common platform for interoperability testing supported by members of the 10GEA XAUI Interoperability Group and the 10 Gigabit Ethernet Consortium
- Full duplex link testing
- 3 link lengths
  - 5 inches
  - 20 inches
  - 34 inches
- XAUI signals run in a system-like environment
  - FR-4
  - multi-layer connections
  - 0.200" backplane thickness
  - MDIO / MDC Support

## Z-PACK HM-Zd

- Fully modular system- standard size is 25 mm
- Available in two versions:
  - 2 signal pairs per column (20 pairs per 25 mm)
  - 4 signal pairs per column (40 pairs per 25 mm)
- Dual beam contact system with fully encompassing grounds
- Robust mating interface with integral prealignment and mating built-in
- Optimized footprint for improved electrical performance



## XAUI Interoperability – Industry Support

The 10 Gigabit Ethernet Alliance has formed a working group, which is chaired by Tyco Electronics, to examine interoperability between different vendors' XAUI implementation. This group selected the Tyco Electronics XAUI HM-Zd Interoperability Platform as a common platform for interoperability testing. The work completed by this group has been adopted by the 10 Gigabit Ethernet Consortium, which will perform future interoperability testing.

Velio Communications, a member of the 10GEA, has tested the XAUI Interface of their VC1003 with the XAUI HM-Zd Interoperability Backplane, and has been able to achieve error free operation at the maximum link length of 34 inches. Velio has summarized this testing in its application support documentation.

For further details regarding the operation of the Velio VC1003 with the XAUI HM-Zd Interoperability Backplane, please contact Bill Woodruff, VP Marketing, Velio Communications, at [bill.woodruff@velio.com](mailto:bill.woodruff@velio.com).

## Velio Communications VC1003

A high-performance, low-power SerDes (serializer/deserializer) backplane transceiver, which can deliver up to 3.125 Gbps over eight full-duplex lanes for an aggregate 50 Gbps on a single device. Consuming 1.9W under typical load conditions, the device can also support 1m of FR4 pc-board trace length plus two backplane connectors, more than double the objectives described in 10-Gbit XAUI (extended attachment-unit interface).

Other devices in the family include the VC1001, an octal SERDES device running channels at 1.25 Gbps and consuming 1.5W, the VC1002, an octal device running channels at 2.5 Gbps and consuming 1.7W. VC1000 devices are available in 25-mm, 380-bump BGA packages.



## Product Summary

2.72 — 3.125 Gbps Eight-Lane CMOS SerDes (Serializer / Deserializer)

*Octal Serdes for 10 Gigabit Ethernet and High Speed Backplane Applications.*

### GENERAL DESCRIPTION

The VC1003 is an eight lane SerDes device targeted for high speed back planes and 10 Gigabit Ethernet applications. Each of the eight lanes is capable of operating in the data range of 2.72 to 3.125Gbps. VC1003 is built using extremely low power and high signal integrity gigabit serial cores developed at Velio communications.

The 8 receivers accept serial data, recover the clock and data, and then deserialize the data into one of several formats, depending upon the configuration. The device is designed for flexibility; it has multiple configuration options, allowing the operation to be tailored to specific system environments.

FEATURES	BENEFITS
Eight 2.72 – 3.125 Gbps SERDES Lanes	Integration conserves board space, reduces power
1.8 V Core Voltage Supply	Low Voltage Core reduces power consumption
1.9 W at 3.125G	Reduces overall system power requirements
CML High-Speed Serial I/O with Programmable Output Voltage Swing	Serial Output Signal can be tailored to specific system conditions
SSTL_2 ASIC-side I/O	Popular I/O standard for flexible ASIC design
Adjustable Pre-Emphasis on Serial Outputs	Reduces Inter-Symbol-Interference, enables serial transmission over longer distances
Typical Receiver Sensitivity as low as 80 mV	Reduces BER on noisy or lossy signals
Compensated On-Chip Termination Resistors for Serial Outputs and Inputs	Internal compensation ensures matched impedances, reducing transmission reflections
8b/10b encoder/decoder (and bypass mode)	Performs 8b/10b encode and decode
10bit/Lane ASIC Interface (10-bit mode) 8bit/Lane ASIC Interface (8-b/10b encoding on the chip)	Multiple bit/Lane modes support 8b/10b and SONET data streams
Self-Test with PRBS Generation	Enables in-system testing and diagnostics
25 mm x 25 mm TBGA	Space-saving, thermally enhanced package

### APPLICATIONS

- 10 Gigabit Ethernet
- SONET Backplanes
- Backplane applications
- Optical Transceiver Interface

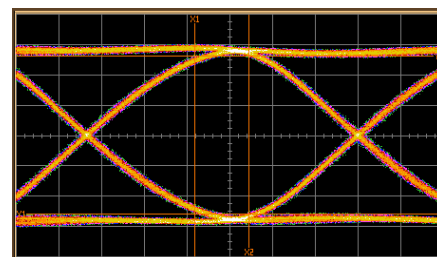
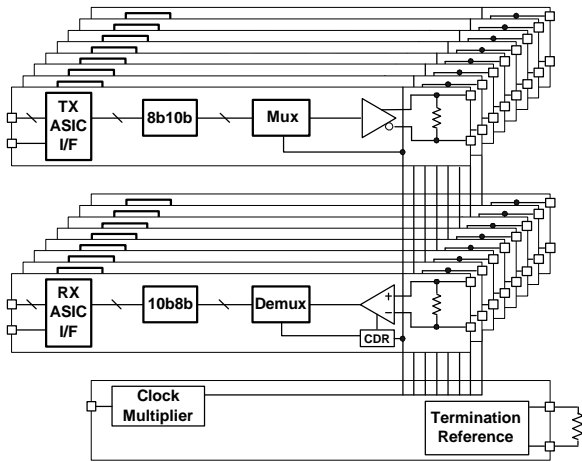


Figure 1: VC1003 Transmit Signal at 3.125 Gbps

FUNCTIONAL OVERVIEW



**Figure 2: VC1003 Block Diagram**

Configurable Serial Outputs for Signal Integrity

The VC1003 utilizes a programmable SERIALizer and DESerializer core for high-speed serial I/O signals. The user-selectable features uniquely address Inter-Symbol Interference (ISI), and help ensure signal integrity at multi-gigabit speeds.

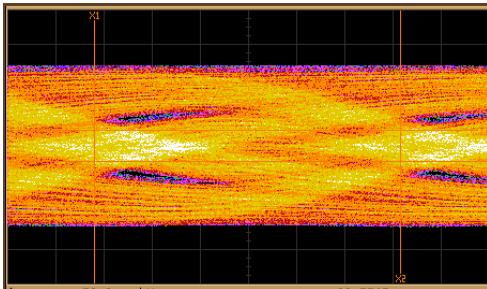
Programmable Pre-Emphasis

To counteract the effects of ISI, the VC1003 serial output signal has an optional pre-emphasis component. This results in a detectable data signal over longer trace lengths.

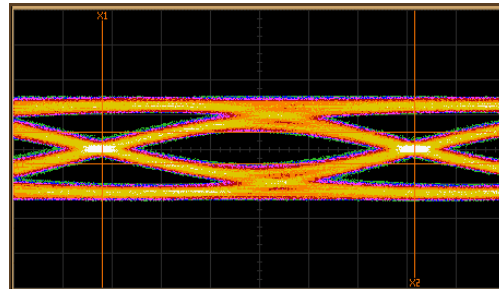
Internal Termination Resistors

Termination resistors are provided on the serial input, as well as the serial output. Input termination resistors are common at these speeds, but the internal output termination deserves special mention. It absorbs reflections from impedance discontinuities, increasing the available signal margin. The value of each of the internal termination resistors is closely matched to that of a single external resistor placed across the RREF+ and RREF- pins.

PRE-EMPHASIS EFFECTS ON SIGNAL INTEGRITY



**Figure 3: 3.125 Gbps Signal Sent Over a One-Meter FR4 Backplane Plus Two Connectors (Pre-Emphasis Turned OFF)**



**Figure 4: 3.125 Gbps Signal Sent Over a One-Meter FR4 Backplane Plus Two Connectors (Pre-Emphasis Turned ON)**

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