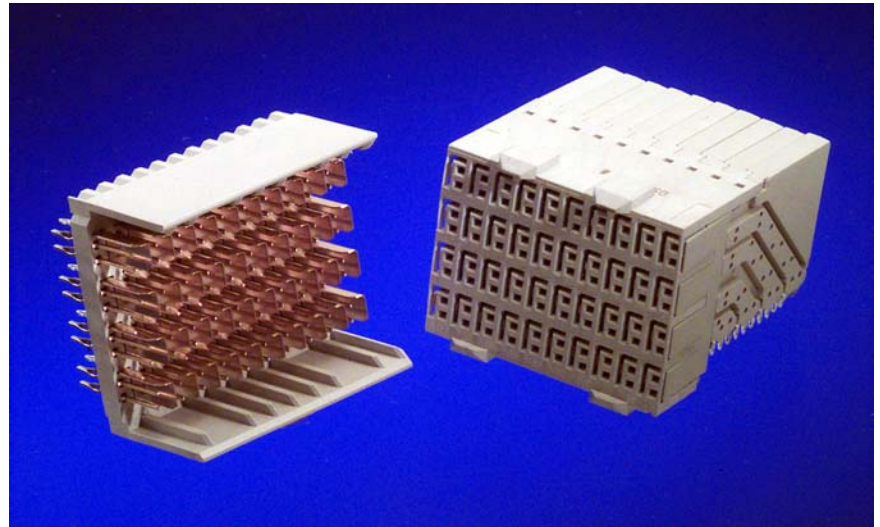


## 10 Gigabit Ethernet

Positioned as a high-speed, unifying technology for networking applications in LANs, MANs, and WANs, 10 Gigabit Ethernet will provide simple, high bandwidth at relatively low cost. In LAN applications, 10 Gigabit Ethernet will enable organizations to scale their packet-based networks from 10 Mbps to 10,000 Mbps, thereby leveraging their investments in Ethernet. In MAN and WAN applications, 10 Gigabit Ethernet will enable service providers and others to create extremely high-speed links at very low cost.



## XAUI HM-Zd Interoperability Platform

- A common platform for interoperability testing supported by members of the 10GEA XAUI Interoperability Group and the 10 Gigabit Ethernet Consortium
- Full duplex link testing
- 3 link lengths
  - 5 inches
  - 20 inches
  - 34 inches
- XAUI signals run in a system-like environment
  - FR-4
  - multi-layer connections
  - 0.200" backplane thickness
  - MDIO / MDC Support

## Z-PACK HM-Zd

- Fully modular system- standard size is 25 mm
- Available in two versions:
  - 2 signal pairs per column (20 pairs per 25 mm)
  - 4 signal pairs per column (40 pairs per 25 mm)
- Dual beam contact system with fully encompassing grounds
- Robust mating interface with integral prealignment and mating built-in
- Optimized footprint for improved electrical performance

## XAUI Interoperability – Industry Support

The 10 Gigabit Ethernet Alliance has formed a working group, which is chaired by Tyco Electronics, to examine interoperability between different vendors' XAUI implementation. This group selected the Tyco Electronics XAUI HM-Zd Interoperability Platform as a common platform for interoperability testing. The work completed by this group has been adopted by the 10 Gigabit Ethernet Consortium, which will perform future interoperability testing.

Utilizing the XAUI HM-Zd Interoperability Backplane, Ixia provides a highly flexible traffic generation and analysis solution for both interoperability and performance testing. The Ixia XAUI Load Modules also provide support for the IEEE 802.3ae Continuous Jitter Pattern (CJPAT) and Continuous Random Pattern (CRPAT). Ixia has successfully proven interoperability with multiple XAUI vendors.

For further details regarding operation of the Ixia XAUI performance verification solution with the XAUI HM-Zd Interoperability Backplane, please contact Charles Bettinelli of Ixia at [cbettinelli@ixiacom.com](mailto:cbettinelli@ixiacom.com).

## Ixia – World's First XAUI Performance Verification

As a principal charter member of the 10 Gigabit Ethernet Alliance (10GEA), Ixia has been instrumental in assisting various XAUI vendors in completing successful performance and interoperability testing. Ixia is offering the world's first and only XAUI tester, which provides highly flexible wire-speed traffic generation and analysis capabilities.

Ixia's XAUI Load Modules are compliant to the latest draft of the IEEE 802.3ae standards and provide additional support for Bit Error Rate Testing (BERT). The XAUI BERT Load Module is programmable to be concatenated for single pattern and statistics over all four channels or channelized for independent patterns and statistics on each of the four channels. The XAUI performance tester is specifically designed to assist developers of Quad SerDes, LAN and WAN PHYs with a XAUI interface, XENPAK transceiver modules and switch and router line cards being developed for XENPAK.

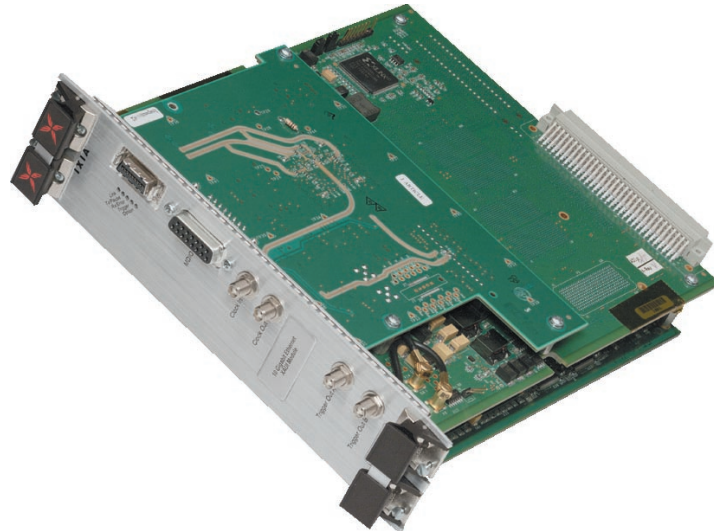
Ixia's family of 10GbE performance verification products also includes 10BASE-SR, 10GBASE-LR, 10GBASE-ER, 10GBASE-LW, 10GBASE-EW and combined OC-192 POS/BERT/WAN optical interfaces.



## 10 Gigabit Ethernet XAUI

Ixia's 10 Gigabit Ethernet XAUI Load Modules offer IEEE 802.3ae compliant wire-speed traffic generation, capture, and analysis for testing Quad SerDes, XENPAK and other devices with a XAUI interface.

The XAUI Load Modules are also configurable for Bit Error Rate Testing (BERT), concatenated for single pattern and statistics over all four channels or channelized for independent pattern and statistics on each of the four channels.



### 10 Gigabit Ethernet XAUI Load Module Specifications

XAUI Tx/Rx Connector Type	Single Fujitsu 8-pair MicroGiga (FCN-268D008-G/1D or /2D)
Clock In/Out Connector Type	2 SMA connectors with clock frequency requirements of 156.25 MHz $\pm$ 100 ppm
MDIO Connector Type	15-pin female D-sub
Transmit Modes	Configurable for Ethernet only, BERT only or Ethernet and BERT modes
BERT Modes	Concatenated for single BER pattern and statistics over all 4 channels or channelized for independent BER pattern and statistics on each of the 4 channels
8B/10B Encoding (BERT)	Software selectable on/off 8B/10B encoding for rates of 2.5 Gbps to 3.125 Gbps
Preamble & Idles	User definable length and content
Capture Buffer	32 MB per port, configurable trigger and filter conditions
Frame Length	Fixed, Random (Specify Min./Max.), Increment from 24 bytes to 64 K bytes in 1 byte increments
Number of Streams	256 (Packet Streams) or 160 (Advanced Stream Scheduler)
Transmit Engine	Built-in FPGA logic for wire-speed packet generation with timestamps, sequence numbers, and packet group signatures
Receive Engine	Built-in FPGA logic for wire-speed packet filtering, capturing, data integrity, and sequence checking
PRBS Patterns (BERT)	2n-1, n={11,15,20,23,31}, All zeros, Alternating Ones/Zeros, 802.3ae K28.5 and K28.7. PRBS can be Inverted as well as User-Defined.
Data Field	All 1s, All 0s, Alternating 1s/0s (by Bit, 2 Bits, Nibble, Byte, 2 Bytes) Increment Decrement, 802.3ae CRPAT and CJPAT, Random, User-Specified
Interframe Gap (per stream)	From 4 ns to 43 sec in 1 byte increments

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## Layer 1 BERT

Industry standard PRBS patterns, counts, and rates enable testing of 802.3ae XAUI physical layer.

## Layer 2/3 Traffic Generation

Data traffic is generated in real time by intelligent logic implemented in FPGAs on each Ixia port. The user can define up to 256 streams. Within each stream, millions of packets can be defined with completely customizable characteristics for every packet header field. Customizable payload contents can also be defined.

## Data Integrity

The data integrity function inserts a signature immediately after the IP header and places a unique CRC at the end of the payload, independent of the frame check sequence. This ensures that the payload is not disturbed as it is passed through the Device Under Test (DUT).

## Sequence Checking

Sequence numbers can be inserted at a user-defined offset in the payload of each transmitted packet. Groups of packets, associated by unique identifiers, can be defined. Upon receipt of these packets through the Device Under Test (DUT), out of sequence errors for each group of packets are reported in real time at wire-speed rates.

## Transmit Scheduler

Wire-speed traffic is generated by Ixia's unique approach to FPGA-based design. User-defined data can be customized and transmitted from each port of the Load Module. There are two modes of transmission available - *packet streams* and *advanced stream scheduler*.

## Packet Streams

The packet streams transmit engine allows generation of up to 256 unique streams on each port. Multiple streams can be defined in sequence containing multiple packets with custom characteristics. After all packets in the first stream are transmitted, control is passed to the next defined stream in the sequence. After the last stream in the sequence is reached, transmission may either cease or control may be passed to any other stream in the sequence. Therefore, multiple streams are cycled through, representing different traffic profiles to simulate Internet traffic.

## Advanced Stream Scheduler

The advanced stream scheduler is a transmit engine that allows generation of up to 160 unique streams. In addition to

defining the standard packet characteristics, an aggregate rate can be defined for multiple streams. The advanced stream scheduler programs the streams to transmit packets in such a manner that satisfies the aggregate rate by scheduling a set of packets to be transmitted from each stream, thus creating a transmission pattern with a mixture of packets with variable rates.

## Interface Connectors

### *XAUI Transmit and Receive*

Eight XAUI lanes, four transmit and four receive, are provided via a single Fujitsu 8-pair MicroGiga connector. In addition, Ixia supplies a single cross-pinned flexible cable assembly, which allows a straight connection between the MicroGiga connector on the Ixia load module and the DUT.



Figure 1. Fujitsu MicroGiga Connector and Cable Assembly

### *MDIO*

A Management Data Input/Output (MDIO) interface is provided to the user via a 15-pin female D-sub connector. The Ixia Load Module acts as the Station Management entity (STA), and can control one or more MDIO Manageable Devices (MMD) in the users system.

### *Clock In/Out*

Two coaxial connectors provide clock input and clock output to allow the user to phase-lock the XAUI interface with the DUT.

### *XAUI SMA Adapter*

Ixia offers a separate box, which connects directly to the cross-pinned cable assembly and separates each XAUI lane into differential pairs via coaxial connectors.

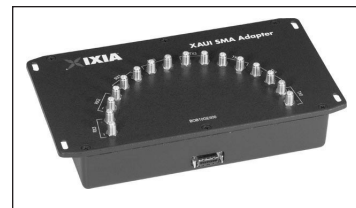


Figure 2. XAUI SMA Adapter

## Product Ordering Information

LM10GE500F1	XAUI Ethernet Load Module, Cable Assembly, Fujitsu MicroGiga Connector
LM10GE500M1B	XAUI BERT Load Module, Cable Assembly, Fujitsu MicroGiga Connector
LM10GE500F1B	XAUI Ethernet and BERT Load Module, Cable Assembly, Fujitsu MicroGiga Connector
BOB10GE500	XAUI SMA Adapter
CON10GE500	Fujitsu MicroGiga Connector

For more information on this product or other available configurations visit Ixia on the web at:

[www.ixiacom.com/products/loadmodules/](http://www.ixiacom.com/products/loadmodules/)