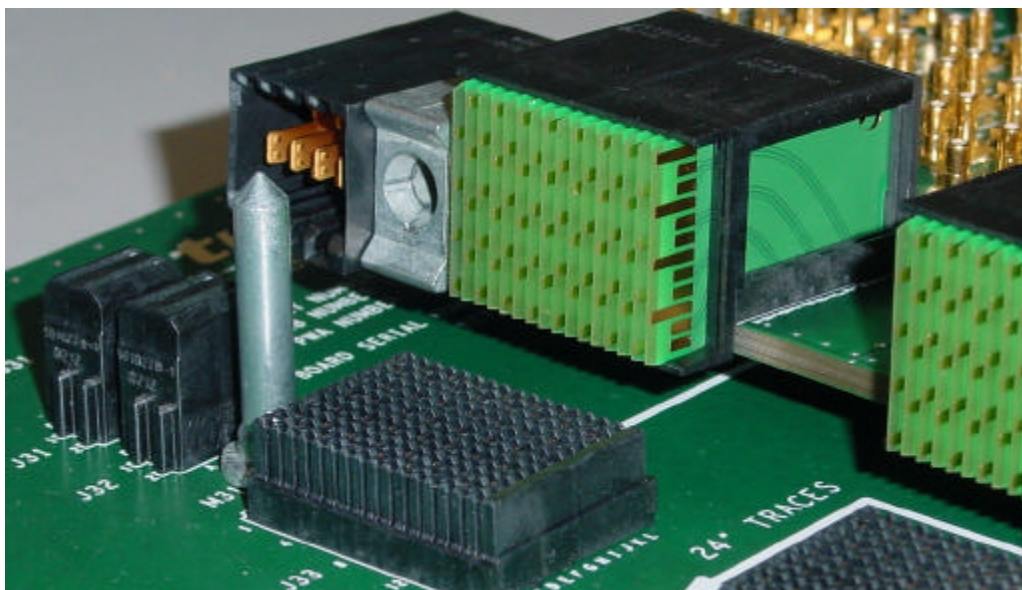




MultiGig RT-2 Connector Routing

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MultiGig RT Connectors

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MultiGig RT-2 Connector Routing

I. INTRODUCTION

As engineers design systems that attempt to push serial speeds across backplane environments in the gigabit per second range, the selection of the system's electrical connector becomes more significant. Electrical, mechanical, and manufacturing aspects of the connector must be considered simultaneously. At the board level these aspects combine with common board design practices to influence the design of the connector-to-board interface and how the board itself will be routed. The manner in which the connector is designed into the system can significantly impact the system's intended performance.

Tyco Electronics has been actively researching these areas in an effort to help customers use the MultiGig RT-2 connector in gigabit serial systems. The combination of interconnect research and intimate knowledge of the connector is presented to provide insight into the capability of a MultiGig RT-2-based system design. Furthermore, this document provides specific design recommendations that will address layout, electrical performance, and manufacturability tradeoffs of the connector at the board level.

II. CONNECTOR OVERVIEW – MULTIGIG RT-2

A. BACKGROUND

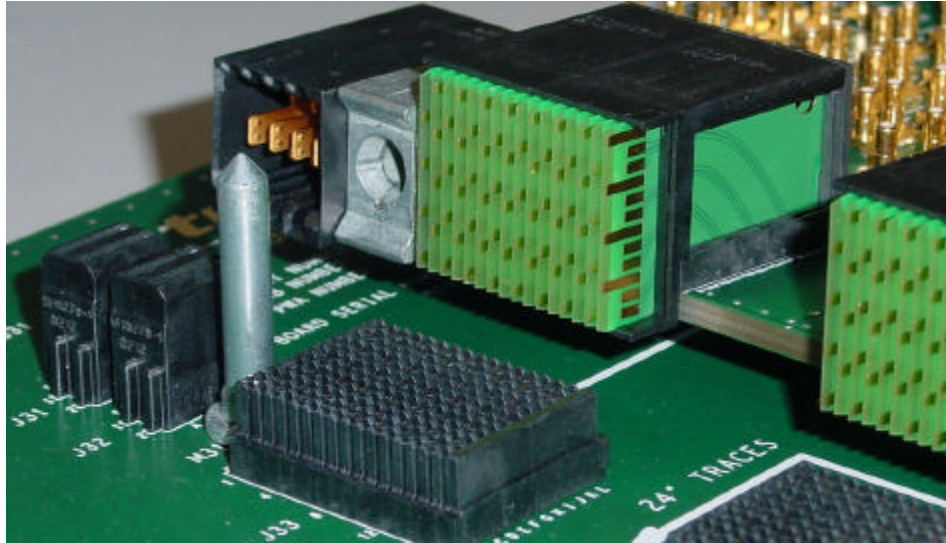


Figure 1: MultiGig RT-2 Daughtercard and Backplane Connectors

Available for both 0.8 inch and 1.0 inch card spacing, the MultiGig RT-2 series is a modular product family allowing freedom to match signal modules, power modules, and guidance, keying, and electrostatic discharge (ESD) options to the needs of the most unique and demanding applications. To extend this flexibility even further, signal modules can be customized for specific electrical and impedance matching requirements.

Outstanding features of the product family include a customizable pinout, large number of guide pin keying combinations, a unique guide pin ESD option, and robust pinless backplane and daughtercard connectors. Both the backplane and daughtercard connectors use industry standard compliant pin technology to attach to PCBs. A unique compliant pin design for all high-speed contacts increases the performance of the connector. Customers have the freedom to customize the sequencing pattern of the contacts to support a variety of electrical requirements.

The MultiGig RT-2 series is ideally suited to high-end applications such as high-speed telecommunications equipment and midrange or high-end servers.

B. FREQUENTLY USED IMPLEMENTATIONS

MultiGig RT-2 is a flexible connector that can be implemented in a variety of wiring patterns. Through the use of a PCB wafer and a generic set of contacts, the wiring pattern for the connector is determined solely by the wafer. This practice allows for differential, single-ended, power, and low-level signaling to be implemented in the same connector without expensive tooling adjustments. The following implementations are most commonly used in MultiGig RT-2 systems. A wide variety of configurations are possible, due to the flexibility of the PCB wafer artwork. Contact your sales representative for details on custom applications with MultiGig RT-2.

1. DIFFERENTIAL

In the differential implementation, the backplane and daughtercard pinouts are shown in Figure 2. The illustrations in this section are specific to the 25.4 mm (1.0") slot pitch part, but are extensible to other slot pitches. Please refer to customer drawings for the specific part you are using for details.

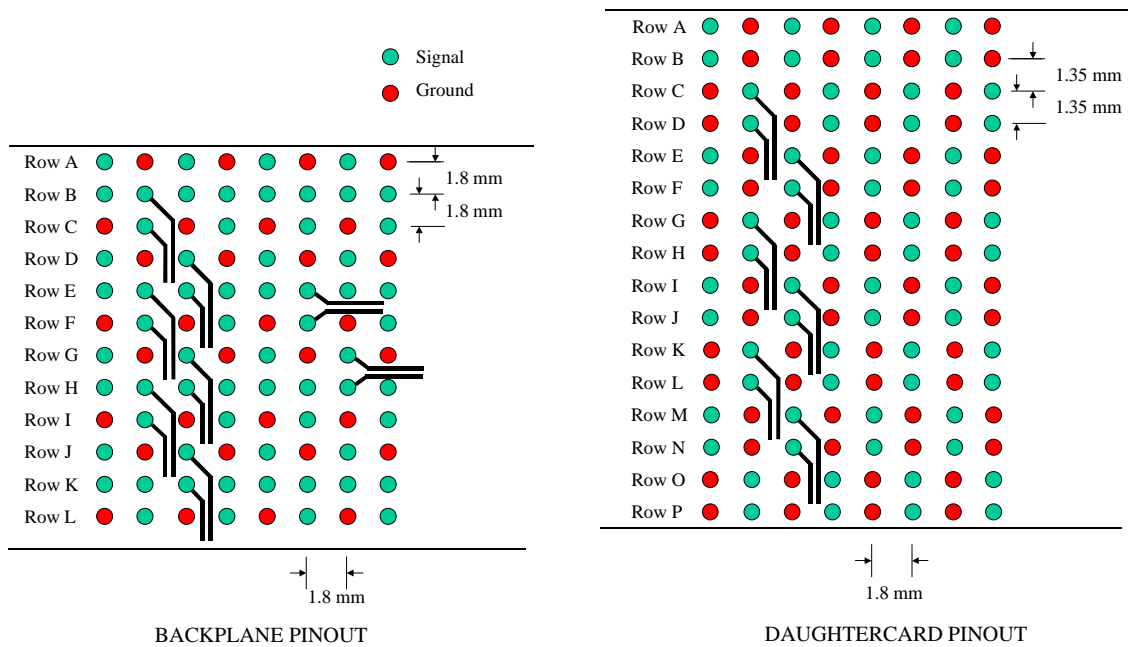


Figure 2: Differential Backplane and Daughtercard Pinouts

Wafers correspond to columns in the connector. Each differential wafer contains four pairs. Two different differential wafers are used in a typical differential assembly to achieve the optimal differential wiring pattern. The daughtercard side of the connector has a 1:1 signal-to-ground ratio, with pairs arranged in a checkerboard-grounding pattern.

Since the pinfields of the daughtercard and backplane contain differing numbers of contacts, due to additional ground pins on the daughtercard, a map is used to determine connectivity for signals between the daughtercard and backplane pinfields. Figure 3 shows the backplane-daughtercard connectivity of odd-numbered columns, and Figure 4 shows the backplane-daughtercard connectivity of even-numbered columns.

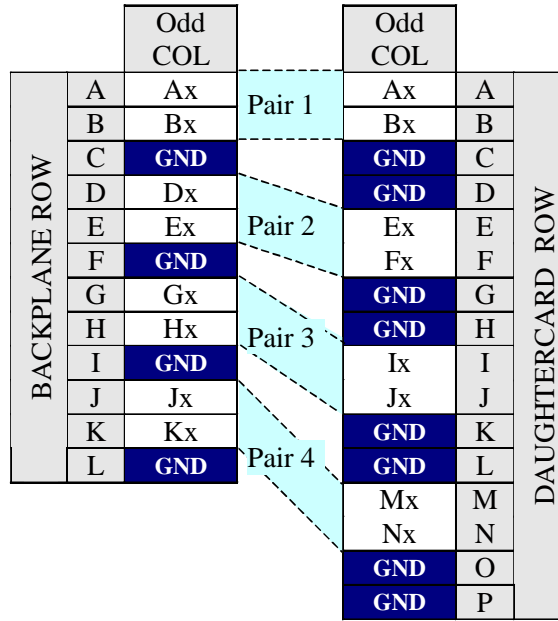


Figure 3: Odd Column Backplane-to-Daughtercard Pin Mappings

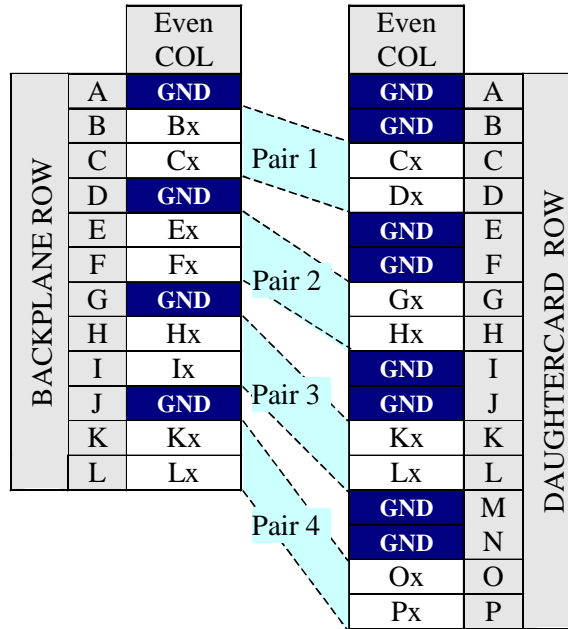


Figure 4: Even Column Backplane-to-Daughtercard Pin Mappings

2. 1:1 SINGLE-ENDED

The most common single-ended implementation of the MultiGig RT-2 connector is the 1:1 single-ended pinout. This pinout is named after the wiring pattern used on the backplane connector. The backplane and daughtercard pinouts are shown in Figure 5. The illustrations in this section are specific to the 25.4 mm (1.0") slot pitch part, but are extensible to other slot pitches. Please refer to customer drawings for the specific part you are using for details.

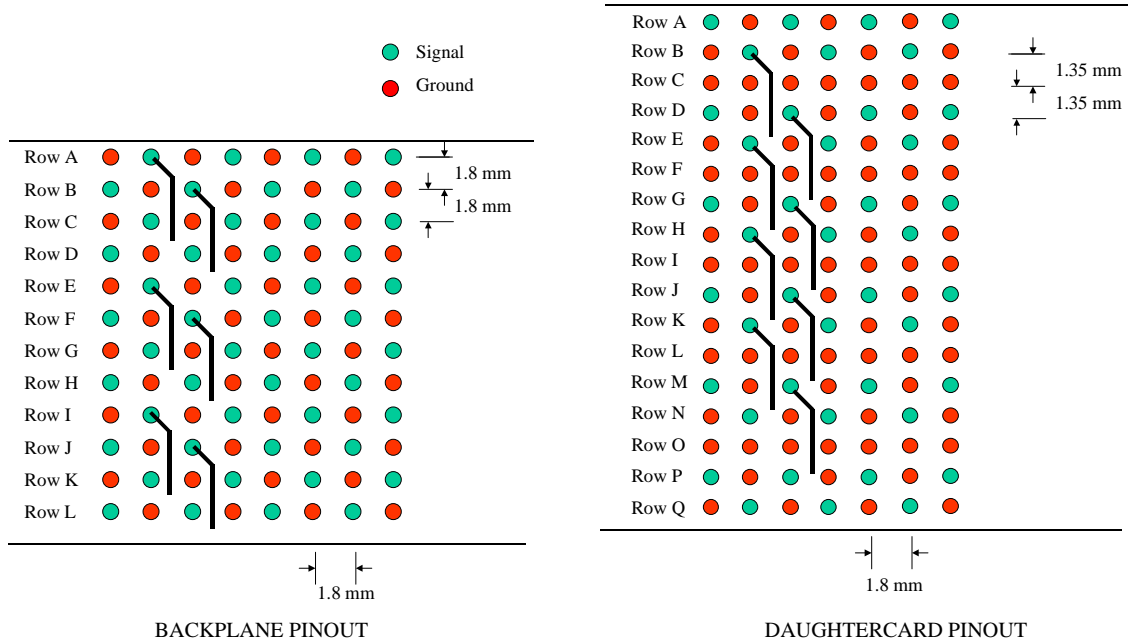


Figure 5: 1:1 Single-Ended Backplane and Daughtercard Pinouts

Wafers correspond to columns in the connector. Each 1:1 single-ended wafer contains six signals. Two different 1:1 single-ended wafers are used in a typical assembly to achieve the optimal single-ended wiring pattern. The daughtercard side of the connector has a 1:2 signal-to-ground ratio, for enhanced performance.

Since the pinfields of the daughtercard and backplane contain differing numbers of contacts, due to additional ground pins on the daughtercard, a map is used to determine connectivity for signals between the daughtercard and backplane pinfields. Figure 6 shows the backplane-daughtercard connectivity of odd-numbered columns, and Figure 7 shows the backplane-daughtercard connectivity of even-numbered columns.

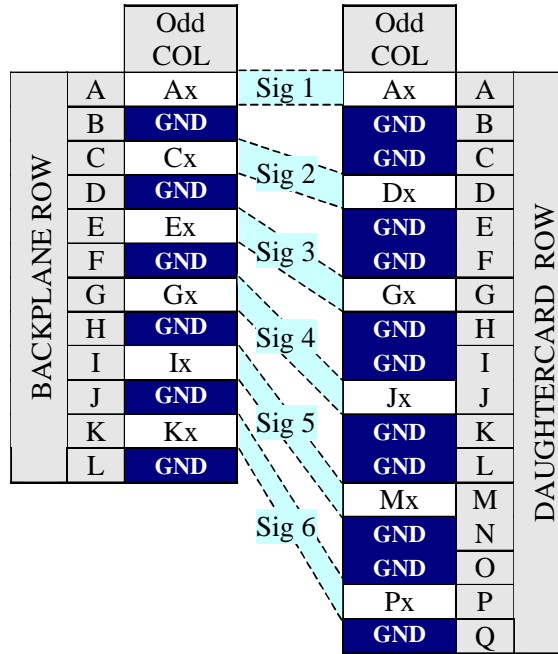


Figure 6: Odd Column Backplane-to-Daughtercard Pin Mappings

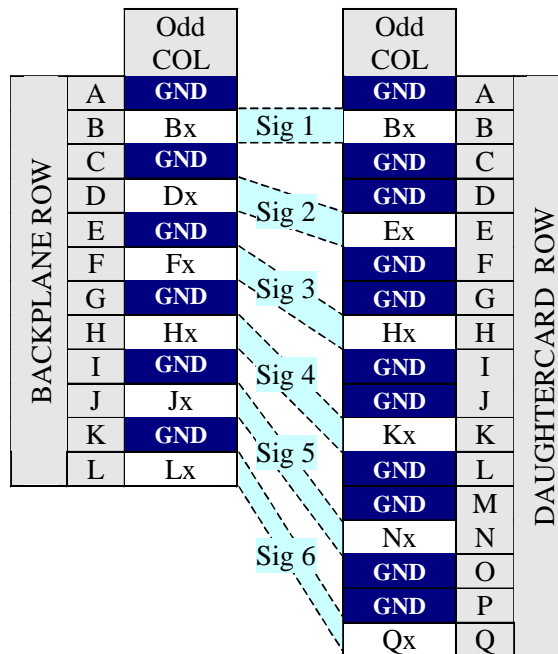


Figure 7: Even Column Backplane-to-Daughtercard Pin Mappings

III. CONNECTOR DEFINITION

A. DRILLED HOLE DIMENSIONS

Full mechanical dimensioning and tolerances are available for all versions of the MultiGig RT-2 connector. These drawings can be located at www.multigigrt.com. The dimensions critical to routing of the MultiGig RT-2 connector are related to the hole pattern, or “footprint”, of the connector. Table 1 is provided to quickly identify critical hole dimensions for the circuit board.

Hole Dimension	Daughtercard Diameter mm (in.)	Backplane Diameter mm (in.)
Drill Hole Size	0.55 ± 0.02 (0.0217 ± 0.0008)	0.65 ± 0.02 (0.0256 ± 0.0008)
Finished Hole Size	0.46 ± 0.05 (0.018 ± 0.002)	0.56 ± 0.05 (0.022 ± 0.002)
Copper Thickness of Hole	0.0375 ± 0.0125 (0.0015 ± 0.0005)	0.0375 ± 0.0125 (0.0015 ± 0.0005)

Table 1: Connector Hole Dimensions

The daughtercard connector for MultiGig RT-2 contains alignment vias that are in addition to the signal and ground vias within the connector footprint. These alignment vias are used during assembly to aid location of the part on the board before the press-fit contacts are seated into the board. These vias should have a finished diameter of 0.56 ± 0.05 mm (0.022 ± 0.002 ”), and can be plated or non-plated.

B. FABRICATION TECHNOLOGY

Other important dimensions for board layout are determined by the capabilities of the circuit board fabricator. Current high-tech PCB industry fabrication technology (i.e. capability) requires minimum pad sizes ranging from D+10 mils through D+18 mils, where “D” is the diameter of the drilled hole size (1 mil, or 0.001”, is 0.0254 mm). For the MultiGig RT-2 connector this results in minimum pad sizes ranging from 0.91 mm (0.036”) to 1.12 mm (0.044”). These resultant pads are the minimum pad sizes required to maintain 0.05 mm (0.002”) of annular ring for a given PCB manufacturer’s capability. Annular ring is an industry standard measure of the clearance between the pad edge and worst-case drill edge after manufacturing. Because the MultiGig RT-2 is typically used in high speed or dense applications where routing issues are most significant, *all pad dimensions in this document will assume a D+12 mil pad size, unless otherwise specified.* The pad diameter may be optimized for specific project needs, and should be evaluated on a project and vendor basis. Designing with a D+10 mil technology PCB could mean reduced yields or breakout, potentially adding cost to the PCB or violating industry specification compliance.

Note: A minimum pad to trace clearance of 0.13 mm (0.005”) will also be assumed for calculating routing dimensions.

1. PAD SIZE

Based upon the D+12 mil fabrication technology assumption, a 0.97 mm (0.038") diameter pad should be used with all MultiGig RT-2 backplane connector pins. On the daughtercard, all signal and ground pins use a 0.86 mm (0.034") pad (based on D+12 technology). For very high-tech PCBs (D+10 mil) the pad is 0.91 mm (0.036") on the backplane and 0.81 mm (0.032") on the daughtercard. In some cases the reduced manufacturability of a D+10 mil technology PCB is required to reduce pad sizes, although potentially reduced yields or causing breakout may add cost to the PCB. Where possible the largest appropriate pad size should be used to provide the PCB manufacturer with the greatest flexibility, thereby reducing overall system costs. Table 2 summarizes different pad sizes for different manufacturing capabilities.

	Pad size				
	High-tech	←—————→			Low tech
	D+10	D+12	D+14	D+16	D+18
Daughtercard Signal & GND	0.81 mm (0.032")	0.86 mm (0.034")	0.91 mm (0.036")	0.97 mm (0.038")	1.02 mm (0.040")
Daughtercard alignment	0.91 mm (0.036")	0.97 mm (0.038")	1.02 mm (0.040")	1.07 mm (0.042")	1.12 mm (0.044")
Backplane	0.91 mm (0.036")	0.97 mm (0.038")	1.02 mm (0.040")	1.07 mm (0.042")	1.12 mm (0.044")

Table 2: Pad sizes for MultiGig RT-2

Thermal reliefs are not required on ground or power pins, because the MultiGig RT-2 connector uses a press-fit technology. A direct connection to reference and power planes will offer the lowest inductance connection to the circuit board.

2. NON-FUNCTIONAL PADS

The removal of non-functional internal pads will improve signal integrity and manufacturability of the PCB. However, some assembly facilities prefer that unused pads are retained in order to maintain hole integrity through various soldering processes. For electrical reasons it is recommended that unused pads be removed on internal layers.

3. ANTIPAD SIZE

Antipads, or plane clearances (Figure 8), are required to separate signal holes from reference voltages to avoid shorting. Choosing the proper size of these clearances is critical in determining several other design parameters: signal integrity, EMI, voltage breakdown, and manufacturability.

Determining the proper antipad size for MultiGig RT-2 depends upon system design goals. Several scenarios are exemplified below.

Antipad sizes are minimized:

- To reduce noise by closely shielding adjacent pins with reference planes
- To reduce EMI by minimizing aperture sizes in reference planes
- To maintain a strong reference to ground for single-ended traces and ground referenced differential traces

Antipad sizes are maximized:

- To maximize voltage breakdown spacing between the pin and the reference plane
- To increase manufacturability by reducing the chance of shorting.
- To reduce reflections in a high-speed gigabit serial system by reducing the capacitive effect of the plated through-hole.

In cases where antipads are minimized, the recommended antipad size is the pad diameter plus 0.25 mm (0.010"). This size maximizes trace coverage, while not risking shorting the plane to the barrel in the case of drill breakout. Using a minimal antipad will increase the capacitance of the via and could degrade system performance at high speeds.

When antipads are maximized, the antipad geometry is dependent on the type of signals passing through the vias. The following sections describe the antipad structures for differential and single-ended signaling, respectively.

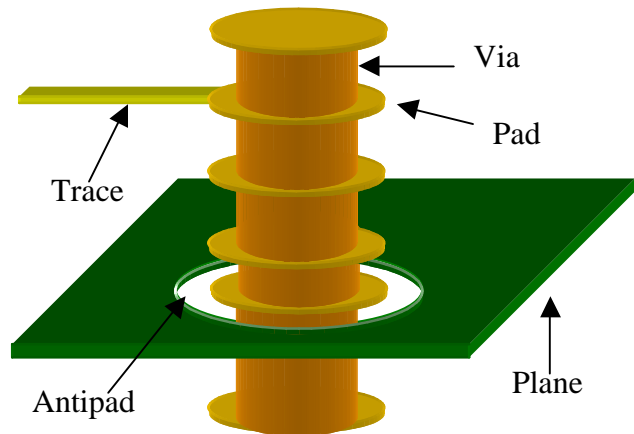


Figure 8: Antipad Illustration

DIFFERENTIAL ANTIPAD STRUCTURES

The differential antipad structure encompasses two adjacent signal vias. This structure minimizes the via capacitance for both vias, while maintaining some coupling between the two signals within the differential pair. The recommended antipad is designed to balance trace coverage and via capacitance. Figure 9 shows the recommended differential antipad dimensions when D+12 pad technology is used.

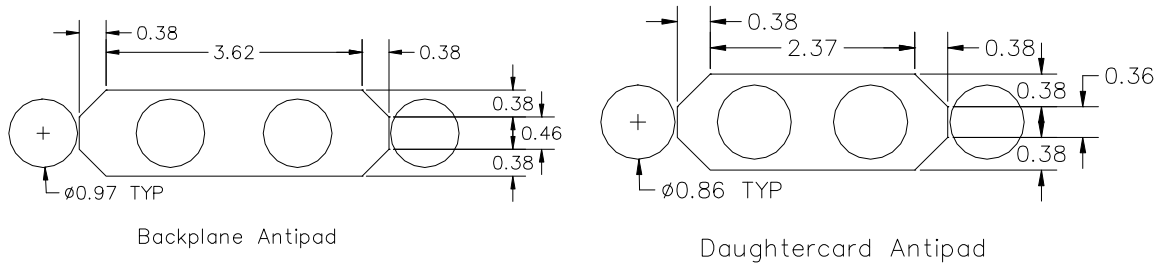


Figure 9: Differential Antipad and D+12 Pad Dimensions

These antipad recommendations are related to the pad size that is used. The antipad height (top-bottom in the above figures) is 0.25 mm (0.010”) bigger than the pad size. In this document, a D+12 pad size is used. Applying these two rules to the Figure 9 example, the backplane pad size should have a 0.97 mm (0.038”) diameter, and the antipad should be 0.25 mm larger, for a 1.22 mm (0.048”) height.

Note that this antipad size assumes that vertical routing will not be used. In cases where vertical routing is needed, a smaller antipad should be used to allow for trace coverage.

SINGLE-ENDED ANTIPAD STRUCTURES

The single-ended antipad structure encompasses only the signal via. Like the differential structure, the single-ended antipad size is designed to balance trace coverage and via capacitance. Figure 10 shows the recommended single-ended antipad dimensions when D+12 pad technology is used.

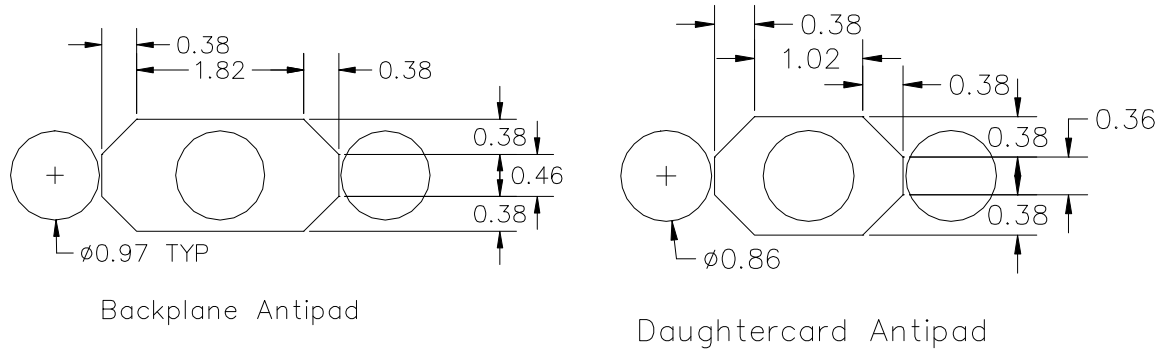


Figure 10: Single-Ended Antipad Dimensions

These antipad recommendations are related to the pad size that is used. As with the differential antipad, the antipad height (top-bottom in the above figures) is 0.25 mm (0.010”) bigger than the pad size. In this document, a D+12 pad size is used. Applying these two rules to the Figure 10 example, the backplane pad size should have a 0.97 mm (0.038”) diameter, and the antipad should be 0.25 mm larger, for a 1.22 mm (0.048”) height.

Note that this antipad size assumes that vertical routing will not be used; in cases where vertical routing is used, a smaller antipad should be used to allow for trace coverage.

C. HIGH-SPEED VIA DESIGN

At gigabit speeds, one of the limiting factors in system design is the effect caused by the via stub in the board. A via stub is the portion of the via that is not in series with the transmission path of the signal, as shown in Figure 11. At high frequencies, this parallel path creates a significant capacitive discontinuity, which degrades the throughput of the link. Although it has a small impact at lower frequencies, this stub typically becomes critical at speeds greater than 3.125 Gbps.

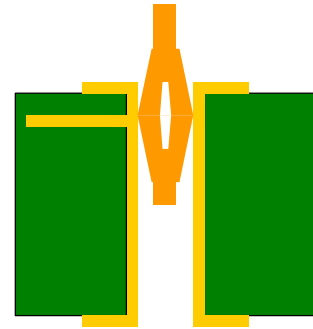


Figure 11 – Via Stub

MultiGig RT-2 was designed to allow for various techniques to be applied to treat the via and remove the stub, without impacting the press-fit contact in the hole. When fully seated, the bottom tip of the eye of needle extends 1.62 mm (0.064”) into the hole on the backplane. The daughtercard eye of needle extends 1.41 mm (0.056”) into the hole on the daughtercard. After this depth, various techniques can be employed to modify the via to eliminate the stub. Consult your board fabrication facility regarding their capabilities for these advanced technologies.

1. COUNTERBORING

Counterboring is a technique that has been used for years by the microwave industry to treat vias in microwave designs. With digital signaling approaching microwave frequencies, similar techniques can be employed to enhance the signal integrity of a link. Counterboring is performed as one of the final steps in the board manufacturing process. After the multilayer board is laminated, drilled, and plated, designated holes are control-depth drilled to remove any via stub that is present. This controlled-depth drill should allow a minimum length of barrel to remain in the hole to allow the eye-of-needle to engage the via. These minimum lengths are given above for both the backplane and daughtercard via patterns. Figure 12 illustrates a counterbored via.

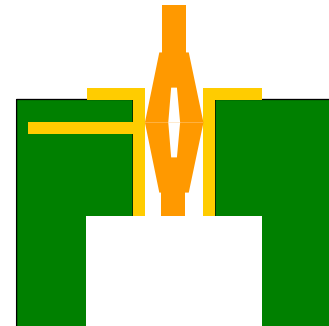


Figure 12 – Counterbored Via

2. BLIND VIAS

An alternative approach that is equally as effective as counterboring is the use of blind vias. Like counterboring, care must be taken to ensure that the depth of the blind via is sufficient to fully engage the eye-of-needle. These minimum depths are given above for both backplane and daughtercard via patterns. Figure 13 illustrates a blind via.

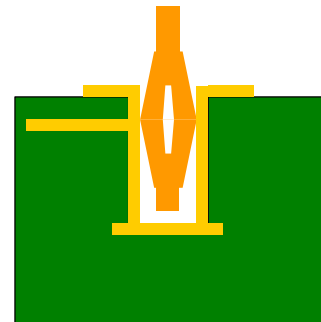


Figure 13 – Blind Via

IV. ROUTING

Because the MultiGig RT-2 connector can be used for both single-ended and differential signals, the routing of both signal types will be examined. Whether routing into or through the MultiGig RT-2 pinfield, the general guidelines are the same.

A. ROUTING CHANNELS

A routing channel is defined by the space between adjacent vias in the connector footprint. In MultiGig RT-2, both vertical (between rows of vias) and horizontal (between columns of vias) routing can be achieved. Typical backplane routing is implemented horizontally, because this type of routing allows for maximal antipad sizes without introducing ground plane voids under signal routing.

Vertical routing is also possible through MultiGig RT-2, but this type of routing should be performed with care to avoid routing over openings in the ground plane. When vertical routing is required, antipads should be reduced to provide appropriate coverage for signals. Note that this practice will increase the capacitance of associated vias and will typically decrease the throughput of those vias. Figure 14 illustrates horizontal and vertical routing techniques.

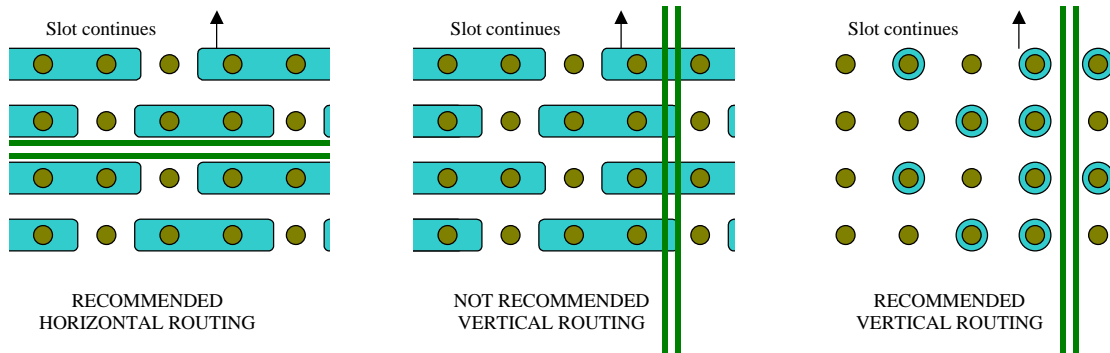


Figure 14: Routing Configurations

B. TRACE WIDTHS

The maximal trace width that can be utilized in a routing channel is a function of the via pitch, the pad size, and the trace-pad clearance. If a D+12 pad size is utilized, the remaining space allows for 7 mil differential lines with 9 mil spaces. Table 3 illustrates the calculation of the available routing channel.

	Metric	English
Via pitch	1.8 mm	0.071"
Pad diameter (D+12)	-0.97 mm	-0.038"
Trace-pad clearance (x 2)	-0.13 mm	-0.005"
	-0.13 mm	-0.005"
Available routing channel	0.58 mm	0.023"

Table 3: Backplane Routing Channel Calculation

For trace width determination, it is also important to ensure that traces have adequate ground coverage underneath them at all times. When routing through the connector footprint, this coverage can be improved by reducing the antipad size on connector footprint vias. However, antipad reduction can result in reduced performance of the via at high speeds. Please refer to section III.B.3 for antipad size recommendations.

C. SKEW & PROPAGATION DELAY

Typical right-angle connectors have differing lengths for the two component signals in a differential pair. In the standard differential MultiGig RT-2 connector, the component signals within a differential pair have been length matched to each other, such that the differential skew within a pair is zero. This feature allows for easy routing of the backplane and daughtercard. In order to have a zero-skew system, length matching within a pair should be used on both the daughtercard and backplane differential routing.

V. ADDITIONAL INFORMATION

A. MULTIGIG WEBSITE

The MultiGig RT-2 connector has an Internet website that contains customer drawings, presentations, and reports on the connector and applications of the connector. Additionally, other connectors in the MultiGig family (MultiGig RT-1, MultiGig power module, MultiGig guide module) can be found at this website. The URL for the MultiGig website is www.MultiGigRT.com.

B. GIGABIT RESEARCH AND GENERAL APPLICATION NOTES

More information regarding Tyco Electronics research into the transmission of electrical signals at gigabit speeds or general application notes are available for download from the Internet at www.amp.com/simulation.

C. ELECTRICAL MODELS

Electrical SPICE and S-parameter models for the MultiGig RT-2 may be requested at modeling@tycoelectronics.com.

VI. CONTACT INFORMATION

The following key contacts can be used to obtain additional information on the MultiGig RT-2 product family.

Technical Support Center	1-800-522-6752	
Brian Burke, Business Development	(717) 986-5340	bfburke@tycoelectronics.com
John Larkin, Product Manager	(717) 592-2074	jtlarkin@tycoelectronics.com
Sam Shaw, Technical Support	(717) 986-5538	sam.shaw@tycoelectronics.com
Brent Rothermel, Signal Integrity	(717) 986-7835	brothermel@tycoelectronics.com